

New Booster LLRF DDS-VME Module

New Parameters and Guidance on Adjusting Them

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RF Outputs

RF 1A: Basic frequency curve plus acceleration phase error feedback.

RF 2A: Same as RF 1A but with “A RF” phase control. (Not Yet Implemented)

RF 3A: Same as RF 1A but with “B RF” phase control. (Not Yet Implemented)

RF 4A: BPM LO Output (SW6 – Up) / Basic frequency curve (SW6 – DN).

- Phase control includes: (Not Yet Implemented)
 - Base phase reference adjusted at transition (90deg before transition -90deg after)
 - Paraphase adjustment including
 - Paraphase Curve run at injection.
 - PC1 offset (PC1OFF) that offsets the paraphase curve vertically throughout the entire cycle.
 - PC2 offset (PC2OFF) that offsets the paraphase curve vertically after the designated number of 1 us updates after the initial Booster Cycle Trigger has been reached (PC2CNT). This is typically set just before **transition**.
 - PBR offset (PBROFF) that offsets the paraphase curve vertically after the designated number of 1 us updates after the initial Booster Cycle Trigger has been reached (PBRCNT). This is typically set near the end of the cycle for the purpose of **bunch rotation**.
 - * *Paraphase adjustments adjust the A RF and B RF sinewave equal amounts in opposite directions.*
 - * *All paraphase functions are disabled if DIP Switch 4 is in the down position.*
 - A RF and B RF phase offset curves. These curves are similar to the frequency curve in that they are defined in ACNET as {time, value} pairs that are interpolated into 1 us updates.
 - RPOS phase shift controlled by an analog phase drive (PSDRV) input. This shifts both the A RF and B RF equal amounts in the same direction.

Digital Inputs, Triggers and Gates

- Trigger Inputs include:
 - **Booster Cycle Trigger (DI_1)**. This triggers the start of the Booster Cycle. This is either a BDOT trigger or a trigger signal with a settable delay from the Booster reset tclk event. Additionally, a Parameter **Curve Delay**, determines how many 20 ns clocks occur between the occurrence of the trigger and the start of the Frequency Curve and Bias Curve playing out.
 - **Transition Trigger (DI_2)**. This trigger signals a paraphase phase shift. A Parameter, X:TRXTIM, determines how long the phase shift takes.
 - **Bunch Rotation Enable Gate (DI_3)**. This gate, in conjunction with the parameter PBRCNT, determines when a paraphase offset is inserted for the sake of bunch rotation near the end of the Booster Cycle. PBRCNT is the number of 1us updates since the start of the paraphase curve that the internal bunch rotation gate goes active. This internal gate AND the Bunch Rotation Enable Gate both have to be active for the bunch rotation offset, PBROFF, to be applied. The Bunch Rotation Enable Gate can be a momentary 1 us pulse since this signal "Sets" an SR flip flop that is reset at the end of the Booster Cycle. With this configuration, the setting of the PBROFF offset is controlled by the particular gate that happens the latest in time.
 - **Beam Valid Gate (DI_4)**. This is equivalent to the current Acceleration Gate signal. This signal is the AND of the Beam Gate which indicates beam in the accelerator and a timed gate signal from ACNET.
 - **Bias Gate (DI_1 rear of VME crate)**. This gates the playing out of the Bias Curve.

Analog Outputs

- Analog Output 1: Scaled representation of the Frequency Curve.
- Analog Output 2: The Bias Curve.
- Analog Output 3: Multiplex Diagnostic Output DAC 3.
- Analog Output 4: Multiplex Diagnostic Output DAC 4.

Analog Inputs

- Analog Input 1: Acceleration phase error feedback.
- Analog Input 2: RPOS Phase Drive feedback. (Not Yet Implemented)
- Analog Input 3: *reserved*
- Analog Input 4: *reserved*

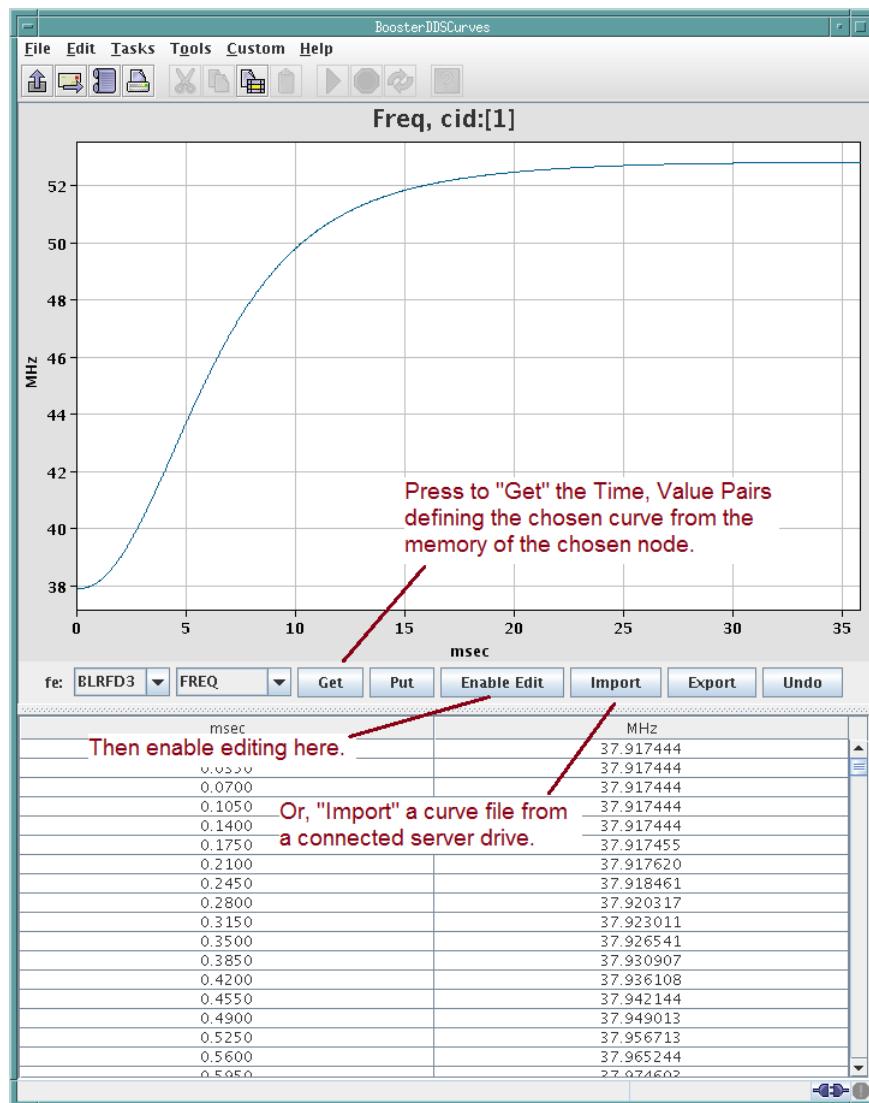
LED Indicators

- X LED: VME Bus Activity
- Y LED: Booster Cycle Triggered (Does not blink in time with the trigger. Will be changed)
- Internal Upper: Acceleration Gate (Beam Gate & ACCEL Gate)
- Internal Lower: *reserved*

Curve Development Application

The Frequency, Bias, Paraphase and Phase Offset curve can be created and edited by the following JAVA program. The current “Booster DDS Curves” application is menu item B129.





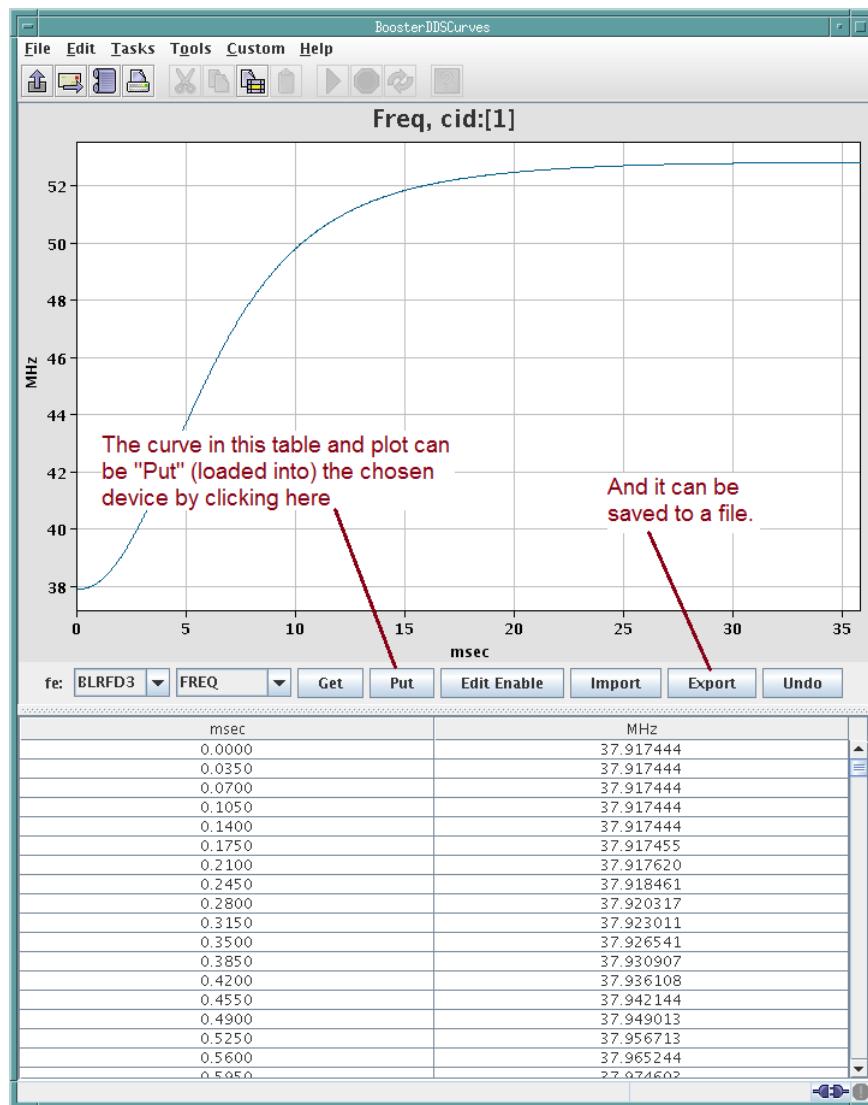


Table 1 ACNET Settable Parameters. (Updated 1/13/2017)

Parameter	ACNET	Legacy ACNET Parameter	Old / New Relationship	Scale Factor	Typical Value	Raw Register Value (hex)
0. Injection Frequency	B:INJFRQ (MHz)	B:VFINJ (MHz)	Same units. A small difference in absolute calibration exists. The new system has a better calibration.	8.94785 Bits/Hz 0.11175869 Hz/Bit	37.933243 MHz	339,420,968 (0x143B2728)
1. No. of Injection Points	B:INJPTS (number of 4 uSec steps)	B:VFIDR (uSec)	Multiply INJPTS by 4 uSec to realize the old units.	Number of 4 us points in curve	80 points	80 (0x0050)
2. Curve Run Delay	B:CRVDLY (uSec)	B:VCDLY (clks)	Relationship is mysterious. Tune CRVDLY in steps of 1,2,5 or 10 uSec.	Micro-Seconds to Number of 20 ns Clocks	100 us	5000 (0x1388)
4. Phase Error Gain	B:PHERGN (positive Integer)	Fixed in old system	Values between 100 and 200 have been found reasonable.	Scale factor 1	180	180 (0x0B4)
5. Transition Trigger Frequency.	B:TTXFRQ (MHz)	B:VTRFTG (MHz)	Adjust in the same manner as old system.	8.94785 Bits/Hz 0.11175869 Hz/Bit	52.213 MHz	467,194,092 (0x1BD8D0EC)
7. Phase Error Trim	X:PHETRM (16 bit offset binary number. 32786 = zero)	No equivalent in old system	Do not adjust.	Is summed with the phase error feedback before gain is applied. (32768 = zero, 16 bit offset binary value). Add 32768 to a value of +/- 32767	32784	32784 (0x8010)
9. Gain Curve Ramp Duration. (<i>Gain can be ramped from zero to the value "Phase Error Gain" linearly over a specified interval</i>)	X:GCDUR	No equivalent in old system	Do not adjust.	Gain curve duration is the interval number times 5.120 us (5.12 = 256 * 0.02)	5.120 us	1

